Second Quarterly Report

LOW COST ARMY MICROMODULE PROGRAM

1 October 1963 to 31 December 1963

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Object of Program

The object of the program is to establish design criteria for development of low cost linear and digital modular assemblies.

Report Prepared By:

P. Margolin
Project Leader

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1.0 PURPOSE

The purpose of the 15-month Low Cost Module Program is to establish design criteria for low cost modules by integrating the best features of the micromodule disciplined geometry packaging technique and microelectronic techniques and devices employing solid silicon, thin films, and hybrid circuits. Projected program objectives are as follows:

(1) Cost Reduction - With the effective packaging of high-population integrated circuits, the price objective in quantity production of Low Cost modules will be less than $5 per circuit, in a module, in quantities of 1000 or more circuits.

(2) Survey — To tabulate the state-of-the-art of thin film and semiconductor solid circuit techniques and the evaluation of their relative potentialities as manifested in off-the-shelf and custom devices. This analysis is to consider the applicability of at least the following specific categories:

a. Availability
b. Cost
c. Logic Circuit Design Method
d. Parts tolerances attainable
e. Frequency capability
f. Environmental effects on stability
g. Reliability
h. Power Dissipation
i. Figure of Merit (mc/mv)
j. Fan-out, fan-in
k. Noise
l. Bias Voltage Levels
m. Versatility
n. Size and Weight
o. Integration costs and techniques

This program takes full advantage of the experience gained by RCA on the Army Micromodule Program and the production facilitations which have been established, as well as the broad basis of support by qualified industries in related programs. Present and

prospective industry suppliers will be used to insure the most effective exploitation of know-how, materials, techniques, and processes developed by industry. The program is equipment-oriented in the sense that practical equipment applications constitute a major input in the decision-making process of device and technique selection.

To achieve the objectives of the Low Cost Micromodule Program, a technical plan consisting of several major concurrent efforts interlaced with a maximum amount of feedback has been implemented. These major tasks are:

(1) Selection of Functional Assembly — Digital and linear equipments are examined to determine the electrical and mechanical requirements for the low cost module. A functional assembly, equivalent to a minimum of 48 standard MICRORAC micromodules, is selected to demonstrate the feasibility of application of a new Low Cost Module to MICRORAC equipment.

(2) Survey and Selection of Devices and Techniques — An industry-wide survey is conducted to obtain a realistic assessment on integrated devices and techniques. Selection is based on suitability to micromodule packaging, cost, reliability, and range of functional performance characteristics.

(3) Design of Functional Assembly — The selected functional assembly is investigated to determine the extent to which the circuits can be adapted to a low cost module. Performance specifications are derived for the assembly.

(4) Fabrication and Test of Preliminary and Developmental Low Cost Modules — The specification derived for a low cost module structure and the specifications for the specific modules obtained from the design investigation of the functional assembly are used to fabricate the required quantity of preliminary and development low cost modules. Sufficient testing is performed to show specification compliance.

(5) Fabrication and Test of Functional Assembly — Development models of a low cost module are used in the construction of the functional assembly to demonstrate the selected function from MICRORAC. Sufficient testing is performed to insure the performance capability of the modular assembly.

2.0 ABSTRACT

The selected functional assembly of MICRORAC, the Timing Level Generator, was analyzed and four module types developed to satisfy its requirements. Of three candidates, Fairchild Micrologic II logic elements were selected over Motorola MECL and Signetics. Six different Fairchild logic elements are used.

A new design module structure called a 28/20-Module assembly was chosen. This module resembles the standard RCA micromodule but has 28 riser wires of which 20 are brought out to serve as plug-in pins. The modules contain either 2, 3, or 4 ICP's and 1 interconnection wafer.

A new Integrated Circuit Package (ICP) having 14 leads was developed as a compatible unit for assembly into the new module. Each terminal of the ICP connects with an alternate riser wire of the module.

Design rules are established for allocating pin functions in the 28/20 module, the ICP's and for employing intra-module riser wire interconnection wafers. Two interconnection wafer types satisfy the requirements of the four module types.

3.0 PUBLICATIONS, LECTURES, REPORTS AND CONFERENCES

3.1 Reports

Packaging comparisons of a 28/20-Module Assembly with other microelectronic approaches were included in a classified missile system study being performed by RCA for the BSD of the Air Force.

3.2 Conferences

3.2.1 Contract Meeting of 24 October 1963

USAEMA and RCA were represented at a third meeting held at Ft. Monmouth, N. J. The subject of this meeting was to resolve an interpretation of SCL 7726 in the light of a preliminary cost comparison study of two alternatives. As a result of this meeting the COTR approved the use of the 28/20-Modular Assembly provided the electronics employed Integrated Circuit packages exclusively.

4.0 FACTUAL DATA

4.1 Introduction and Background

4.1.1 Functional Assembly

The study of the MICRORAC computer led to the selection of the "Timing Level Generator" as the demonstration vehicle for "Functional Assembly".

4.1.2 Integrated Electronics Devices

In the area of device selection, illustrating the application of integrated electronics to MICRORAC, the field was narrowed to three candidates, i.e., Fairchild-Micrologic, Motorola-MFCL, and Signetics 100 series.

4.1.3 Logic Contents of a Module

The determination of the logic contents of a module and the number of module types awaited the decision of the device selection.

4.1.4 Module Structure

A module structure was selected which would have 28 internal riser wires of which 20 emerged from the bottom face.

4.1.5 Lead Frame

Two candidates, a 12-terminal and a 14-terminal lead-frame were under evaluation.

4.1.6 Interconnection Wafers

A 28 notch interconnection wafer was proposed as a preliminary design.

4.2 Functional Assembly

4.2.1 Analysis of Functional Assembly

The timing Level Generator (TLG) function is distributed over an equivalent of more than one MICRORAC Booklet. A tabulation of the logic used in the TLG is as follows:

Diode Cluster	1 (3 input)
Modified Gate	14
Standard Gate	22
Non-Inverting Power Amplifier	16

Jam Gate	1
Flip-flop	11
Power Amplifier	18

The MICRORAC modules used in the TLG consist of the following combinations:

Module Type	Logic Contents
Gate	2 Standard Gates or 2 Modified Gates
NPA	1 Non-Inverting Power Amplifier and one 3-input Diode Cluster
Jam	1 Jam Gate and 1 Standard Gate
FF	1 Flip-flop
PA	1 Power Amplifier and one 2-input diode cluster.

To perform the function of the TLG, the following micromodules are required:

Micro-Module Type	Quantity Required
Gate	18
NPA	16
Jam	1
FF	11
PA	18
TOTAL	64 micromodules

This leaves the following circuits for use in implementating the logic in parts of the computer other than the TLG.

Three-Input Diode Cluster	15	Equivalent to 18 micromodules
Standard Gate	1	
Two-Input Diode Cluster	18	

A maximum of 23 logic micromodules and one filter capacitor are allowable on a MICRORAC printed board which gives a total of 46 logic modules and 2 capacitor modules per booklet. The unused logic circuits can fill 18 micromodules. The Timing Level Generator logic exceeds the logic contents of one booklet (two printed boards) and more than meets the contract requirements. At the same time it has the advantage of being a functionally complete unit.

The Timing Level Generator is essentially a four flip-flop binary counter with routing gates to effect either a 10 or 12 count in a code designed so that only one bit of four changes state at any count. Each count is decoded to form a timing level which is used throughout the computer to direct the logical operations. Additional logic is provided to permit continuous operation via an external clock or step-at-a-time operation with an external one-shot multivibrator.

In addition to the 10 or 12 basic timing levels, there are five extended timing levels also incorporated into the TLG.

4.3 Integrated Electronic Devices

As described in the introduction, the list of candidates for use in the demonstration unit was narrowed down to three on the basis of published data. These are:

Fairchild Micrologic

Motorola MECL

Signetics 100 series

The three candidates were examined on the basis of price, propagation delay, noise margin, pin requirements, logic flexibility, and power requirements.

4.3.1 Prices

100 UP Prices-$/Flat Pack

	Fairchild	Motorola	Signetics
Basic Gate	$17.40	$37.00	$44.75
Flip-flop	22.30	43.00	64.75
Average Price of Logic Line	29.84	37.00*	52.22

Thus, Fairchild Micrologic is the choice on the basis of price alone.

The Texas Instruments series 53 devices were excluded because only tentative data sheets have been received and availability at this time is questionable.

*Excluding Bias Driver which is not a logic element.

4.3.2 Propagation Delay

The propagation delays of the three units were compared on a small laboratory test setup constructed of four gates loaded with capacitance. Two of the gates were separated by about two feet of twisted pair wire of the type used in the MICRORAC computer. The setup is shown in Figure 2 of the first quarterly report. The results are presented in the chart below. Three values of capacitance loading used per stage were as follows:

Test 1. No added capacity; just that associated with the connectors, interconnecting wires, etc. This is less than 10 pf per stage.

Test 2. C = 120 pf - Approximately the worst case loading capacity for a MICRORAC gate with a fanout of five.

Test 3. C = 240 pf. An arbitrary doubling of the above value to get an idea of the effect of heavy capacitive loading.

Basic Gate Propagation Delay Per Stage

	No Added Capacity	C = 120 pf	C = 240 pf
MICRORAC DM1364	25 nsec	48 nsec	60 nsec
Fairchild 903	15	24	34
Motorola MC306F	7.5	20	34
Signetics SE101K	38	81	125

These results show the Signetics integrated circuit to be slower than the MICRORAC micromodule circuit in the mechanical configuration used. The Signetics unit was dropped, largely on the basis of this test. The Signetics connection used in this test has the two voltages and the internal collector resistor connected. This gives maximum speed and maximum power dissipation.

4.3.3 Noise Margin

A noise margin and noise susceptibility test was performed on the various devices. A more extensive study than that performed here is desirable but such testing would require more time than the program schedule permits. These tests are of crucial significance in making a selection between various devices.

The following chart shows some noise factors for the three type units under consideration:

	Inductive Noise Margin	ΔI (Fanout = 5)	F^1_{NM}	Capacitive Noise Margin
Fairchild	0.2v	3.2 ma	0.063	0v
Motorola	0.4v	1.5 ma	0.267	0.4v
Signetics	0.6v	7.5 ma	0.080	2.8v

Inductive noise may be represented by the relationship

$$e = M \frac{dI}{dt} = M \frac{\Delta I}{\Delta T}$$

where M is a function of the interconnection wiring. Since M is fixed for a given computer and the induced voltage must be less than the noise margin, a figure of merit expressed as $F_{NM} = V_{NM} \times \frac{\Delta T}{\Delta I}$ should be maximized, where V_{NM} = the difference between the worst case induced voltages and the minimum voltage required to change the state of the driver element.

A simplifying assumption is made that ΔT (the rise time of the loop current) is the same for all three devices. This follows if the same circuit loop is used for all three devices. The circuit loop impedance is more likely to determine loop current rise time than the actual device switching time.

The fixed ΔT is incorporated into a modified Figure of merit $F^1_{NM} = \frac{F_{NM}}{\Delta T} = \frac{V_{NM}}{\Delta I}$.

F^1_{NM} is shown for the devices under consideration in the third column of the Table; the highest number is the most desirable.

A corresponding capacitive figure of merit is dependent on the h_{FE} of the integrated transistors; there is no information on hand on this. In this condition the driving transistor is off and the driven unit is on. The noise margin figures given in the fourth column of the Table do not indicate that the Fairchild unit is useless, rather that any capacitively coupled noise immediately appears at the base of the transistor. However, the effective overdrive and charge storage of the transistor must be taken into account before a definitive statement can be made about this condition.

In addition to the two conditions considered above, the case of current hogging must be considered. This is where a stage is coupled to several other stages, and because of tolerance buildups, one stage receives minimal drive, or currents must be rapidly switched, despite such a condition, through the series inductance of interconnecting leads. Motorola units are not subject to this problem, whereas Fairchild and Signetics units are.

In summary, a brief analysis shows the Motorola MECL units to be superior in noise characteristics to Fairchild and Signetics units. However, the comparison with the present MICRORAC circuits must take into account any differences in wiring layouts. This must await further investigation.

4.3.4 Pin Requirements

The number of pins that must be interconnected is a significant factor in the use of integrated circuits. Where the device is mounted directly on printed boards, the lead concentration about the module mounting location can get inconveniently high, resulting in crosstalk and conductor tolerance problems. The number of integrated circuit flat packages that can be mounted in modules is limited by the terminal pin density. Since flat package thicknesses are generally 0.06 inch, fifteen or more integrated circuits could be easily stacked within a module one inch high. However, the fixed maximum number of 20 pins severely limits the number of devices that can be placed in a package. This leads to the conclusion that a fewer number of pins is a desirable feature of an ICP. The pin requirements for each of the three devices under consideration are given below:

	No. of Pins Required
Fairchild	6
Motorola	9*
Signetics	8

On a pin basis alone, Fairchild would be the clear choice. This factor will be discussed further in Section 4.5.1.

*A non-complementing output is available as a tenth pin.

4.3.5 Logic Flexibility

The range of logic devices made by the three manufacturers differ. The differences are best illustrated in chart form:

	F	S	M
Three Input Gate	X		X
Four Input Gate	X	X	
Five Input Gate			X
Dual Two Input Gate	X	X	
Gate Expander	X	X	X
Power Gate	X	X	X*
Flip-flop	X	X	X
Shift Register Element	X**	X**	
Counter Element	X		
Half Adder	X		X
One Shot		X	

F = Fairchild, S = Signetics, M = Motorola

*The Motorola power gate is the standard gate which has high fanout capability.

**The Signetics shift register element is a complete stage in itself whereas the Fairchild shift register element requires two elements per stage.

The fan-in and fan-out for the three basic gates are:

	F	M	S
Fan-out	5	26	5
Fan-in	27	25	34

The Motorola unit has the additional advantage of having a noninverting output. The Fairchild unit has a disadvantage of a complicated set of rules for reducing fan-out for different loading combinations. The Signetics and Motorola units offer an advantage, in that their outputs can be tied together to form a Virtual-OR logic function, thereby saving logic gates and reducing propagation delay.

In general, none seems to be clearly superior or inferior to the others when compared on a basis of logic flexibility.

4.3.6 Power

The nominal power dissipations of the basic gates are as follows:

	Power (mw)	
	ON	OFF
Fairchild	19.2	6.9
Motorola	3.7	36
Signetics	12.7	6.0
MICRORAC DM1364	87	43

Thus, on the basis of power alone, Signetics units are the logical choice, although all dissipations are less than for the MICRORAC circuits.

4.3.7 Summary

The above comparisons are summarized in the Table below. In each case the numbers indicate order of choice.

	F	M	S
A. Price	1	2	3
B. Propagation Delay	2	1	3
C. Noise Invulnerability	3	1	2
D. Pin Requirements	1	3	2
E. Logic Flexibility	-	-	-
F. Power	2	3	1

A final choice of the Fairchild Micrologic was made. The propagation delay requirement eliminates the Signetics candidate. There is no significant difference in logic flexibility, and since the power dissipation of both Fairchild and Motorola devices is below the equivalent micromodule gate, only a slight advantage is held by the lower power Fairchild unit. The speeds of the two devices are roughly equivalent and satisfactory. Of the remaining three criteria, Motorola holds an advantage in noise invulnerability, whereas Fairchild has the advantage in price and pin requirements.

As indicated before, the noise study is not yet conclusive and more work remains to be done in this area. Also, the major goal of this program is low cost, and in both remaining criteria, cost and pin requirements, the Fairchild unit will effect savings. The smaller number of pins will allow more integrated circuits to be mounted in a micromodule, thereby realizing packaging efficiencies that can be translated into cost savings because the MICRORAC would require a fewer number of modules.

4.4 Differences Between Present MICRORAC Logic and Fairchild Micrologic

The devices used in the MICRORAC Timing Level Generator are given in Section 4.2.1. The devices are:

Standard Gate — This is described as a positive NAND. Let the inputs be designated as A, B, and C, and the output D. For positive circuit logic a low (or ground) corresponds to a bar over the symbol and a symbol with no bar indicates a high (or +4.5v) signal.
Thus,

$$\overline{D} = ABC \text{ (positive logic)}$$

then by DeMorgan's Theorem

$$D = \overline{A} + \overline{B} + \overline{C} \text{ (positive logic)}$$

Diode Cluster — Used to increase the number of inputs to a gate.

Modified Gate — This is a Standard Gate without a collector resistor. In practice, the collectors of a Standard Gate and a Modified Gate are connected directly together to form a Virtual OR. In Boolean terms, let the inputs to the Standard Gate be A, B, and C with an output D, and further let the input to the Modified Gate be E, F, and G with the same output D. Then, the output is low if either or both of the two gates has all three inputs high. Therefore,

$$\overline{D} = ABC + EFG$$

And again by DeMorgan's Theorem

$$D = \overline{ABC}\ \overline{EFG}$$

Power Amplifier — This is the logical equivalent of the Standard Gate with a greater fan-out capability.

Non-Inverting Power Amplifier — This is a non-inverting positive AND gate with a large fan-out capability. If the inputs are designated H, I, and J with the output K, the Boolean expression is

$$HIJ = K$$

and

$$\overline{H} + \overline{I} + \overline{J} = \overline{K}$$

Jam Gate — This circuit is used exclusively in conjunction with the Flip-flop with a Jam input. It has a clock input and a data input. The circuit will set the flip-flop to the state indicated by the data input at the time the clock pulse is present.

Flip-Flop — Bistable circuit.

The Fairchild Micrologic devices proposed for use in the construction of the Timing Level Generator are:

Buffer Element (900) — This is used as a simple inverting circuit with a large fan-out capability. If the input and output are designated as L and M respectively, the Boolean expression is

$$M = \overline{L}$$

Flip-Flop Element (902) — Bistable circuit.

Three-Input Gate Element (903) — This is the basic gate. Logically it is equivalent to the MICRORAC Standard Gate. It differs in its polarity however, in that this is a positive NOR and a negative NAND. In order to demonstrate the logical identity with the MICRORAC, the opposite convention from that used previously for the MICRORAC circuits will be used. That is, a bar over a symbol indicates a high (or +3.0v) signal, whereas a symbol with no bar indicates a low (or ground) signal. Designating the inputs as N, O, and P and the output as Q, the Boolean expression becomes

$$\overline{Q} = NOP \quad \text{(Negative Logic)}$$

$$Q = \overline{N} + \overline{O} + \overline{P}$$

Half Shift Register Element (906) — This is a set-reset flip-flop with two integrated two-input gates, one driving each of the flip-flop inputs. Each of the gates has a distinct data input and a common gating input.

Four-Input Gate Element (907) — This is the same as the three input gate except for an additional input lead.

Dual Two-Input Gate Element (914) — This device consists of two independent two-input gates each identical with the three-input gate except for one less input lead.

There are several places in the MICRORAC Timing Level Generator logic where the Virtual OR operation described on pages 13 & 14 is used. This connection is not available with the Micrologic and must be duplicated another way. One method uses four gates. Consider the first two gates with input A, B, C at one gate and E, F, G at the other. Then we have two outputs, $\overline{ABC}$ and $\overline{EFG}$. Each output is then fed into an input of a two-input gate, giving:

$$\overline{\overline{ABC}\ \overline{EFG}} = ABC + EFG$$

This is passed through an inverter whose output

$$D = \overline{ABC + EFG} = \overline{ABC}\ \overline{EFG}$$

which is the same expression as that given for the MICRORAC circuit on pages 13 & 14.

There is no equivalent to the Jam Gate in the Micrologic system. However, the logic can easily be accomplished by using gating through two separate gates into the set and reset inputs of a flip-flop.

4.5 28/20-Module Assembly and Structure

4.5.1 Module Structure

This study has shown that the pin limitation is the severest impediment in mounting integrated circuits in modules. In addition in order to hold down the cost it is necessary to have as few lead cuts as possible. (A lead cut is a break in the micromodule vertical riser wire so that two connections may be made to the same riser wire with electrical isolation between the two.)

In the assembly of a group of integrated circuits into a module an advantage accrues when using a group of circuits with only one supply voltage and ground. To show this, consider first a group of circuits with two supply voltages and ground. If more than one circuit of a type is to be mounted in a module, a maximum of two circuits could be accommodated without cuts or the use of more than one pin per voltage. The possibilities are:

(1) Two voltages or one voltage and ground brought out of centerline riser wire positions with the third lead connected to one of the corner riser wires. Here 180° rotation about the centerline axis is the only other connection. A unit with one supply voltage and ground can locate up to a theoretical maximum of four circuits in a 28/20 module assembly without cuts or the use of more than two external pins.

(2) Two voltages and ground all brought out to (3) corner riser wires. With eight corner riser wires only 2 positions of the integrated circuit module are possible.

The above discussion shows the advantage of Fairchild Micrologic over the other two devices under consideration when integrated circuits are to be mounted in the 28/20 module assembly.

The next question concerns the manner in which the logic leads of the integrated circuits are connected. There are two alternatives:

(1) All logic leads brought out independently to pins, or

(2) Some logic lead interconnections made within the micromodule.

Considering the second possibility first, it is impractical to generate special modules by interconnecting the same type differently within a micromodule. Let x and y represent circuit pins of one circuit and subscripts 1 and 2 represent different circuits. If x_1 and y_2 are brought out to a common pin, it necessarily follows that x_2 and y_1 must be connected to another common pin, which is rarely desirable. Since a large number of digital computer circuit interconnections are serial gate connections without feedback, this eliminates a large number of intra-module interconnections.

The next possibility for connections within a micromodule is between integrated circuits of different types. Some advantage can be gained in this type of connection, and in a computer design it would be necessary to study the logic to determine an optimum

set of interconnections. One immediate possibility is driving at least one flip-flop input with a gate output. There may arise some restrictions because each circuit must be used with several types of other circuits, and a lead frame designed for interconnection with one type of circuit must not interfere with mounting and interconnection with other circuits in other micromodules.

Six lead frame layouts were completed covering all types of circuits required for the Timing Level Generator using Fairchild Micrologic. The six types are described in Section 4.4. Four micromodules were designed with these circuits (see Figure 4-1).

Table 4-1 shows the make up of each module type in terms of the logic and interconnection water elements. Table 4-2 shows the allocation of the 28 riser wires for use of V_{cc}, GND and signal leads. Each Fairchild logic element is plotted on the table. Also shown is the 4 positions of an ICP which are possible, with the selected lead allocations. Figure 4-2 illustrates the 4 positions of ICP's in a 28/20 module assembly. The eight corner leads are used for V_{cc} and ground only. These service leads are brought to an emerging terminal pin via an interconnection wafer.

4.5.2 Figure 4-3 shows an exploded view of the various parts comprising an ICM module. In this module four 14-lead ICP packages and one wafer are assembled with a combination interconnection-end wafer and so the wafer serves as an interconnection medium; it ties the ends of the riser wires and eliminates all internal cutting of riser wires. The active leads of the ICP packages are indicated with numbers. All inactive leads are shown in phantom.

In this design the interconnection pattern and end wafer have been combined to minimize interconnection tie-points. In this case the overall module height is approximately 0.45 inch high.

In the design and development of a 20-lead header with provisions for 28 internal riser wires, three basic approaches are explored as follows: A hermetic-sealed header, an epoxy or thermo-setting plastic header, and a modified version of the present micromodule. In the first two cases, preliminary specifications have been furnished various manufacturers for cost projections, as well as establishing a source within the time frame of the contract requirements. The advantages and disadvantages of a complete

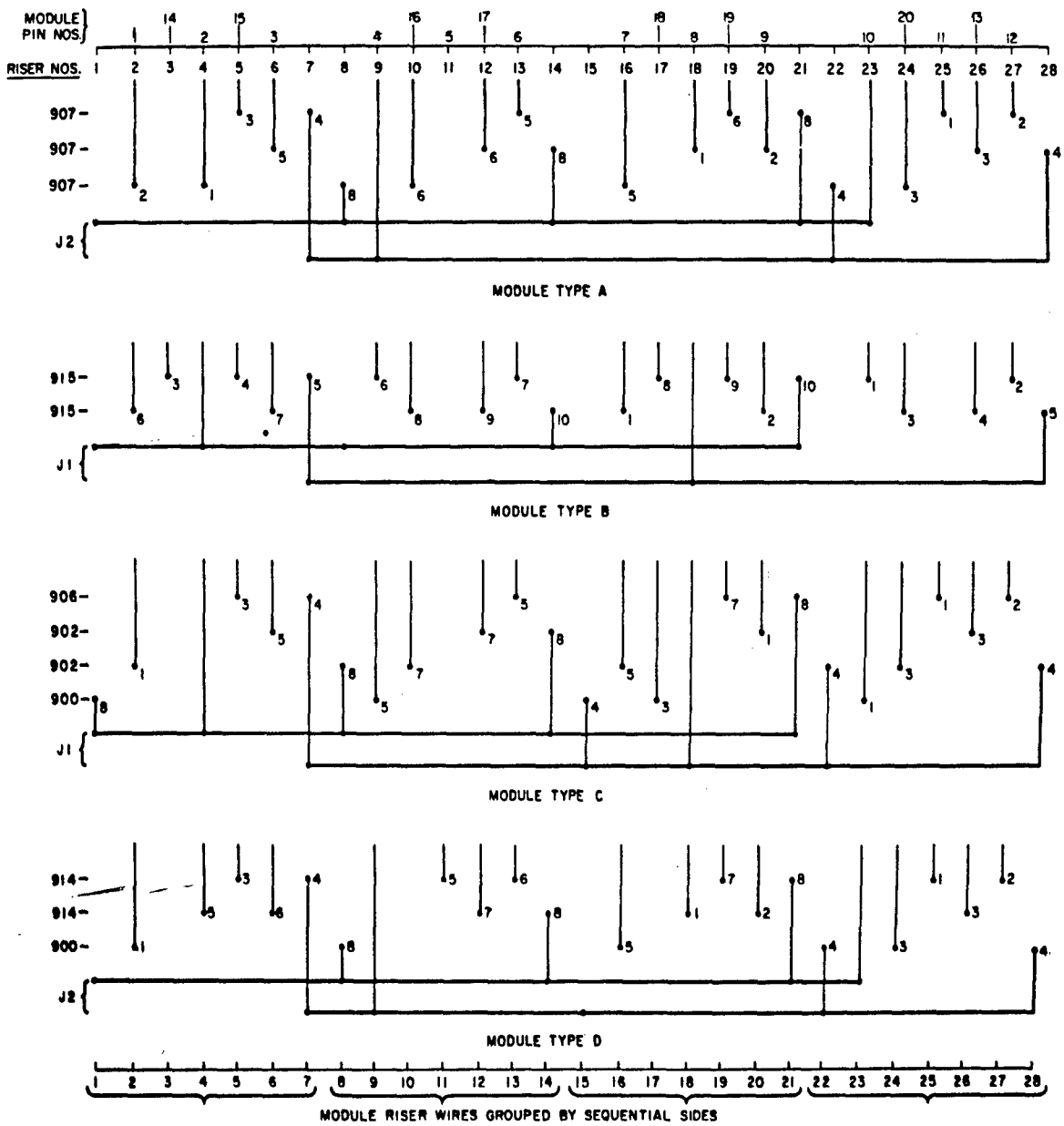


Figure 4-1. Module Interconnections

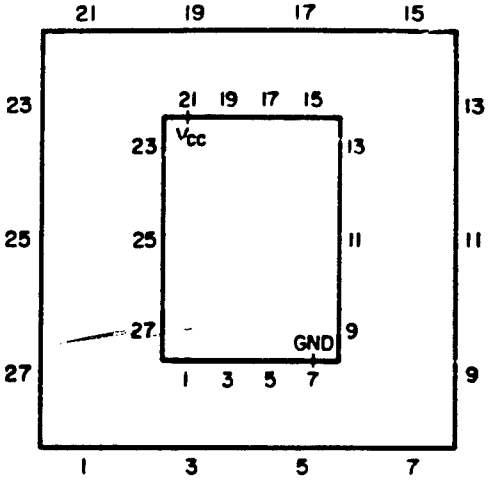
TABLE 4-1. 28/20 MODULE LOGIC AND INTERCONNECTION WAFER

MODULE TYPE	QUAN USED IN TLG*	FAIRCHILD ICP'S QUAN	TYPE	FUNCTION	INTERCONNECTION WAFER QUAN/MODULE	TYPE
A	4	3	907	4-INPUT GATE	1	J2
B	8	2	915	DUAL 3-INPUT GATE	1	J1
C	5	1	906	HALF SHIFT REGISTER (WITHOUT INVERTERS)	1	J1
		2	902	FLIP-FLOP		
		1	900	BUFFER		
D	6	2	914	DUAL 2-INPUT GATE	1	J2
		1	900	BUFFER		
TOTAL	4 TYPES	23 MODULES		6 ICP TYPES		2 WAFER TYPES

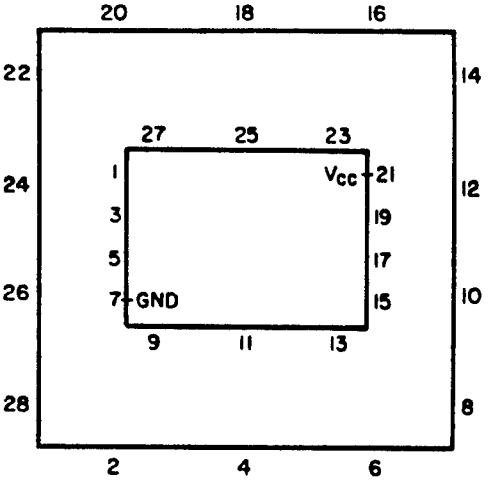
* TLG - TIMING LEVEL GENERATOR (MICRORAC)

Table 4-2. ICM Risers and ICP Terminals with Corresponding Fairchild Logic and Voltages

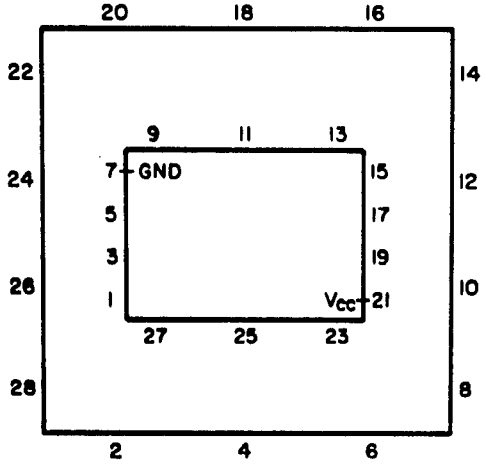
POSITIONS USED						POSITION (1)		POSITION (2)	POSITION (3)	POSITION (4)
1,2	1,2	1,2,3	1	2,3	3,4	REF				
FAIRCHILD MICROLOGIC						RISER	ICP TER-	90° CL	FLIP ICP	90° CL
915	914	907	906	902	900	WIRE NO.	MINAL NO.	ROT. ICP	ABOUT 4-18	ROT. ICP
		V_{cc}				1	1			21 V_{cc}
						2		9	27	
3-C						3	3			19
						4		11	25	
4-D	3-C	3-C	$3\text{-}B_0$	$3\text{-}B_0$	3-A	5	5			17
						6		13	23	
5-GND	4-GND	4-GND	4-GND	4-GND	4-GND	7	7 GND			15
		V_{cc}				8		15	21 V_{cc}	
6-E						9	9			13
						10		17	19	
	5-D					11	11			11
						12		19	17	
7-F	6-E	5-D	$5\text{-}B_1$	$5\text{-}B_1$	$5\text{-}B_2$	13	13			9
		V_{cc}				14		21 V_{cc}	15	
		GND				15	15			7 GND
						16		23	13	
8-G						17	17			5
						18		25	11	
9-H	7-F	6-E	$7\text{-}A_1$	$7\text{-}A_1$	$7\text{-}B_1$	19	19			3
						20		27	9	
$10\text{-}V_{cc}$	$8\text{-}V_{cc}$	$8\text{-}V_{cc}$	$8\text{-}V_{cc}$	$8\text{-}V_{cc}$	$8\text{-}V_{cc}$	21	21 V_{cc}			1
		GND				22		1	7 GND	
1-A						23	23			27
						24		3	5	
	1-A	1-A	$1\text{-}A_0$			25	25			25
						26		5	3	
2-B	2-B	2-B	2-P	$1\text{-}A_0$	$1\text{-}R_1$	27	27			23
		GND				28		7 GND	1	



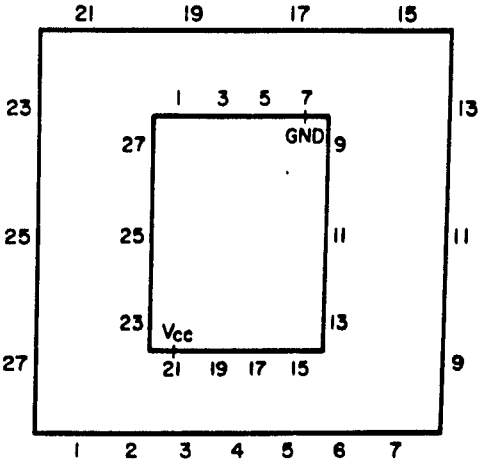
REFERENCE POSITION (1)



POSITION (2)
(90° CL ROTATION OF ICP)

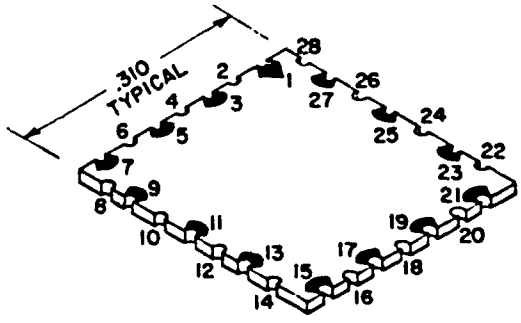


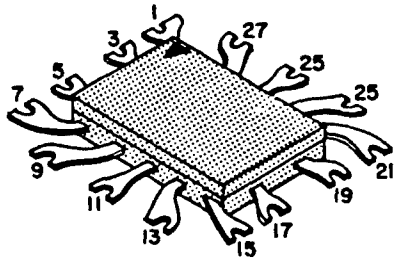
POSITION (3)
(FLIP ABOUT 4-18 OF ICP)



POSITION (4)
(90° CL ROTATION OF ICP)

Figure 4-2. Graphical Illustration of (4) ICP Orientations in a Module





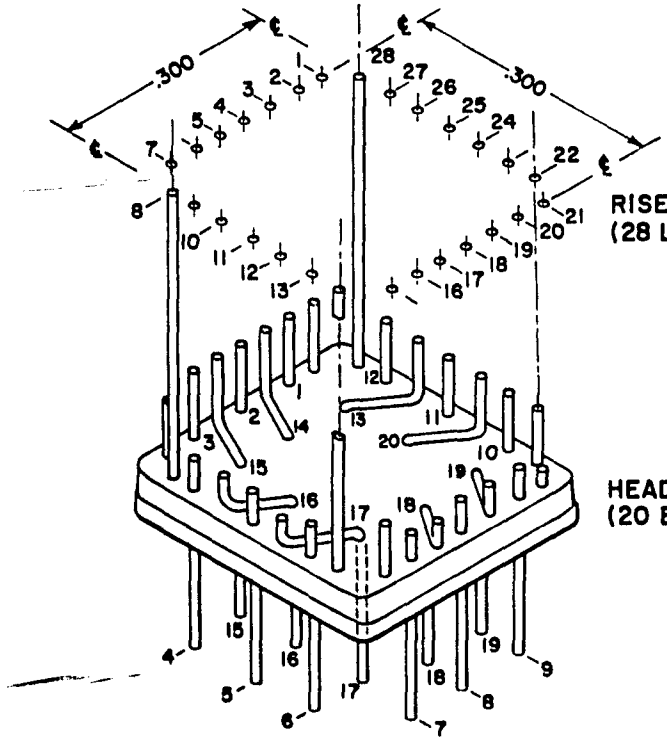


Figure 4-3. 28/20 Integrated Circuit Module (ICM): Exploded View Showing Internal Construction

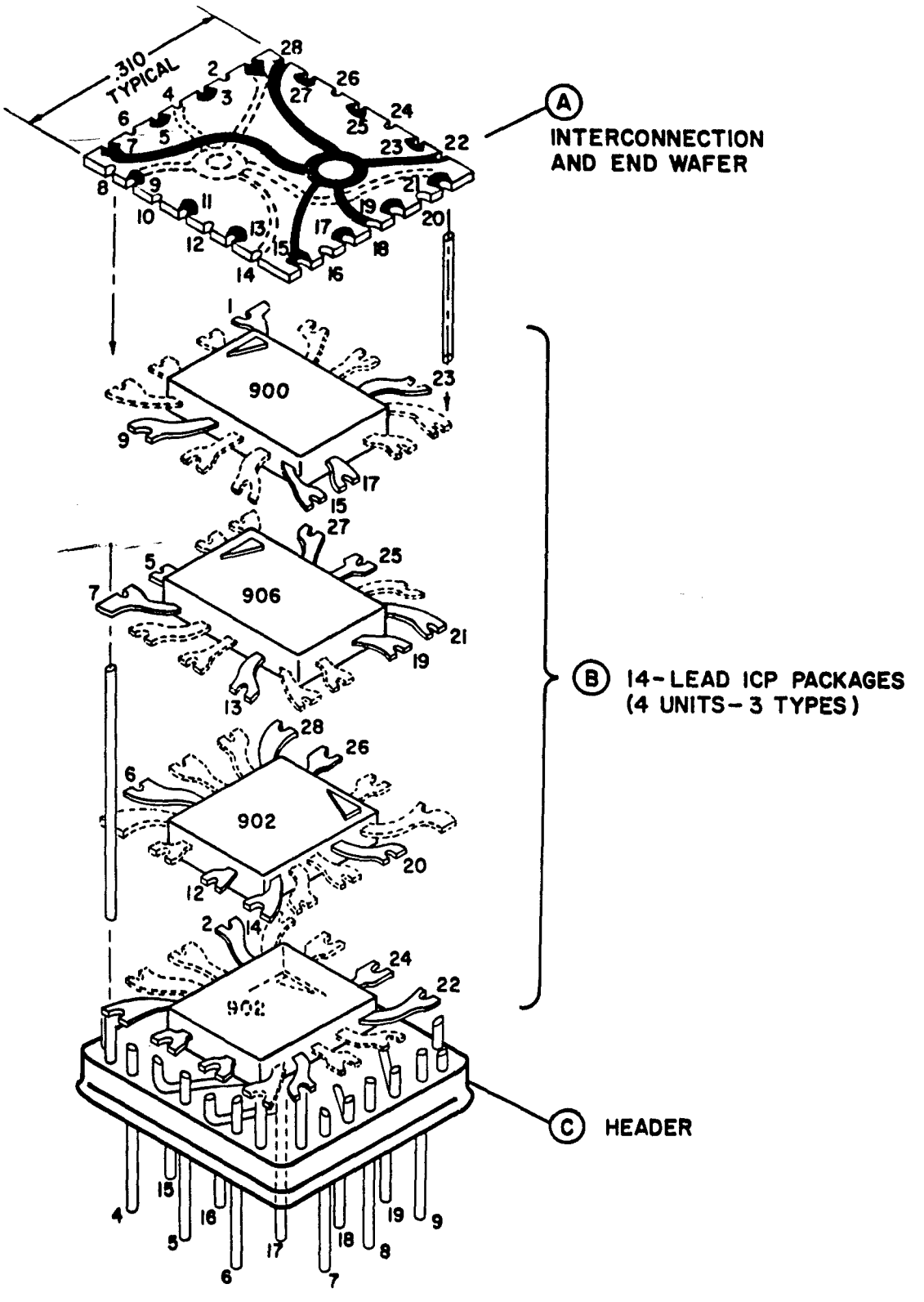


Figure 4-4. Typical ICM Construction Showing Assembly Sequence of Four ICP Packages

hermetic-sealed unit in place of the encapsulated module are being reviewed relative to cost, tools, fabrication complexities, etc. The 28/20 Module Assembly will require a modified shell enclosure (to accommodate 20 leads) and necessitate bending of 8 internal terminations after soldering operation. In this case the encapsulation procedure is similar to the micro-module.

Miscellaneous items as metallic can enclosures, equivalent extruded type epoxy skirts or shells, 20-lead module sockets and/or related jig fixtures are, likewise, being investigated.

4.5.3 Lead Numbering - Topology

Lead orientation of the various parts of a typical three-dimensional Integrated Circuit Module (ICM) is shown in Figure 4-4. The exploded view shows the sequence of assembly: the header, the integrated circuit package (ICP) and a typical end-wafer or microelement substrate. The header comprises 20 external leads and 28 internal riser wires. When viewed from the plug-in end the leads are numbered clockwise - 1 to 12 on external perimeter and 13 to 20 on internal perimeter. The inside surface of the header (viewed down) is numbered counterclockwise - 1 to 28 inclusive (representing the internal riser wire cage). The ICP package comprises 14 terminations or spider leads - numbered counterclockwise (top view) as shown. The 14-lead pattern of the ICP package is compatible with manufacturing design and processes of various vendors' flat package configurations. This permits assembly of an ICP package with soldered connections to tie points of alternating position in each plane normal to the riser wire cage assembly.

Similarly, the end wafer or microelement substrate is numbered clockwise on the bottom (counterclockwise on the top). It is important to note that there is no direct correlation of the numbering sequence of the various integral parts of the ICM Design and is only illustrated here to establish a clearer pictorial relationship of the assembly process. To facilitate usage for equipment assembly, each ICM Module will be identified as to specific type and will bear a marking indicating the No. 1 riser wire with leads numbered in a clockwise sequence.

4.5.4 Other Considerations

As part of the 28/20 module design concept the following special features are being considered:

(1) The development of a practical technique, which simplifies the dip-soldering process of the wafer stack at assembly and minimizes "bridging", is being investigated.

(2) Such provisions as a mechanical polarization at the module level and an access hole to facilitate removal from the printed circuit board (similar to the MICRORAC Design) may be incorporated as part of this task.

4.6 Compatible Integrated Circuit Flat Package (ICP) Mechanical Design

4.6.1 A 14-lead ICP was derived by using alternate positions of a 28 riser wire module cage. Leads exiting from the ceramic body follow a 4:3:4:3 sequence. If lead 1 of the ICP connects to riser wire 1 of the module assembly then all ICP leads will contact odd numbered riser wires. A 90° rotation of the ICP will contact all the even numbered riser wires.

The 28/20 Module Assembly employs a compatible ICP having 14 leads. A single lead pattern is arranged to contact alternate riser wires in the module. All 28 risers can be contacted by using two ICP's where one is rotated 90° from the first.

In practice, a maximum of nine of the 14 are required (to accommodate Fairchild's 915 Dual 3 input gate). Six types of Fairchild Micrologic II elements Figure 4-7 shows the variations of Monolithic Silicon logic elements, made by Fairchild, inside a standardized flat package which is made compatible with the 28/20 Module Assembly.

The 14 lead Integrated Circuit Flat Package design is shown in Figure 4-5. The construction techniques of the Fairchild ICP configuration utilizes a kovar lead frame. The view shows the lead frame removed for clarity. The flat package is approximately 0.060 inch thick, 0.250 inch long by 0.175 inch wide. The 14 leads or spider array match the 28 lead riser wire positions (0.0375 grid) of the module header.

The geometry permits package rotation and flipping within the caged riser wire harness, thus optimizing a potential eight different positions for each ICP. Based on logic and service lead selection a maximum of 4 positions are possible without introducing module wire cuts.

FIG.___. 14-LEAD INTEGRATED CIRCUIT FLAT PACKAGE (ICP)

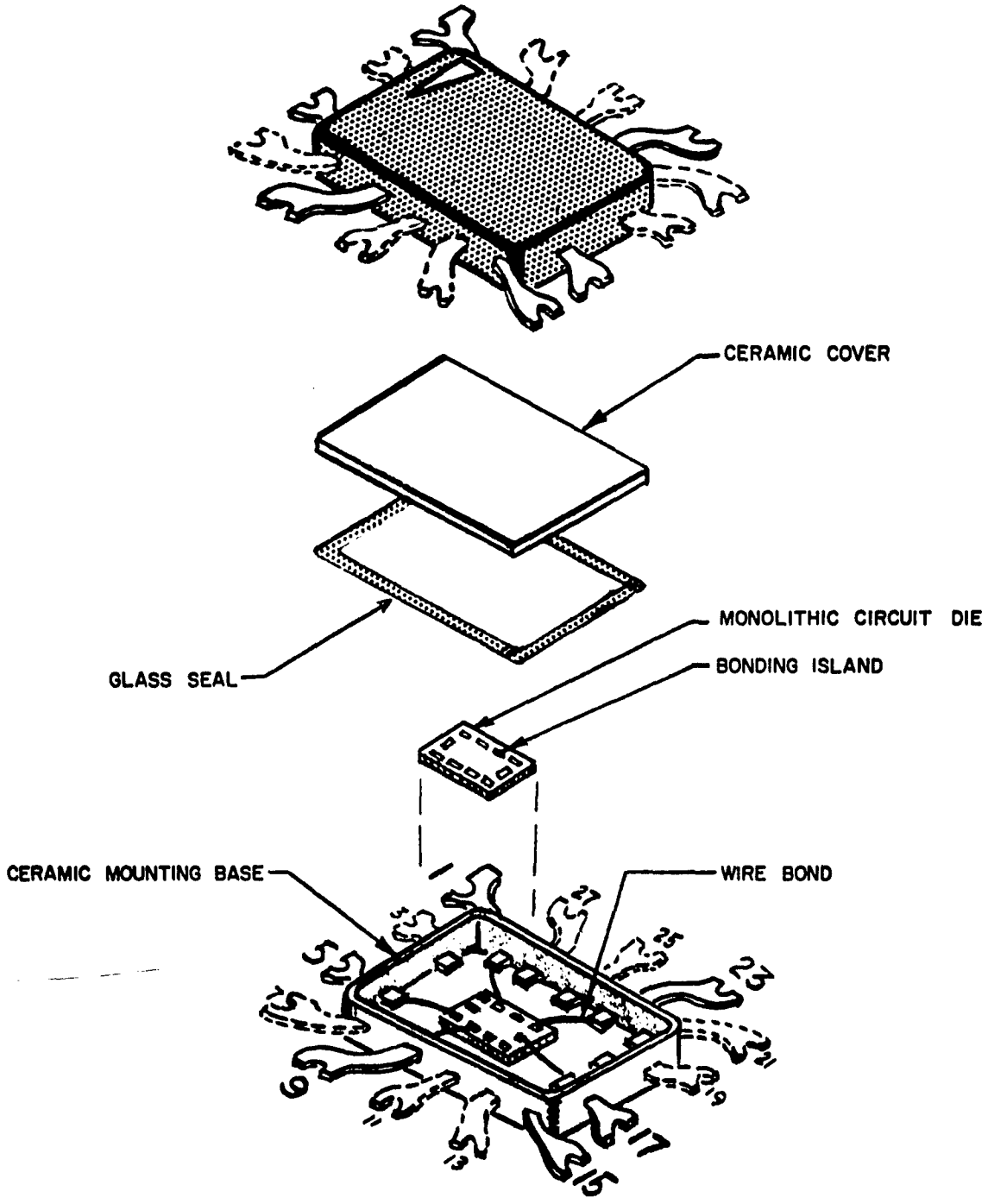


Figure 4-5. 14-Lead Integrated Circuit Package

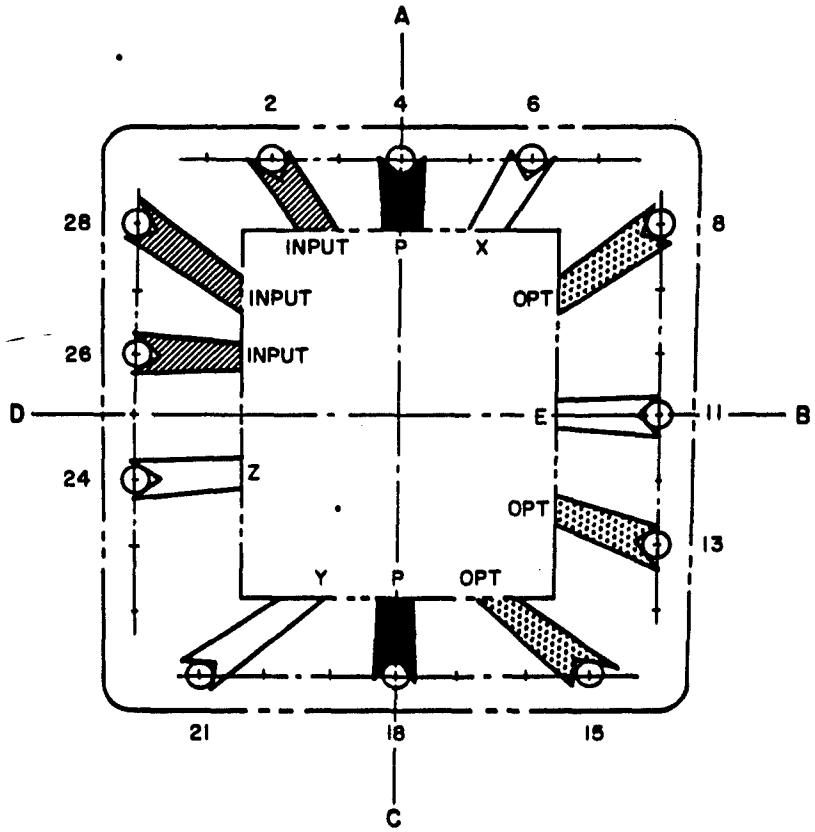


Figure 4-6. 12-Lead Integrated Circuit Flat Package

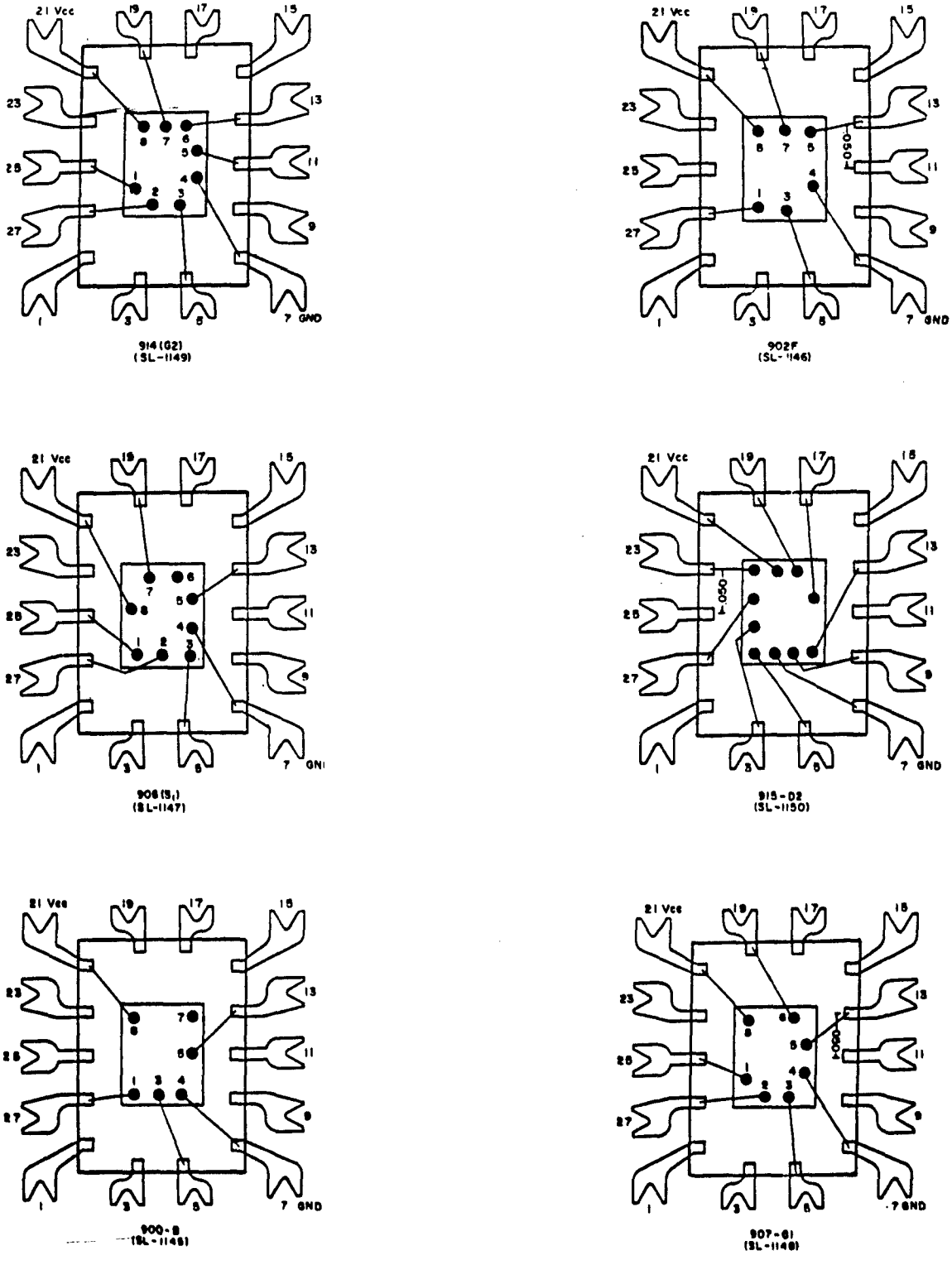


Figure 4-7. Six ICP's Showing Internal Lead Bonding Arrangement

A 12 lead integrated circuit flat package configuration, Figure 4-6, was considered, but did not provide sufficient assembly flexibility. This pattern consists of both even and odd terminations as shown. The 12 lead package layout provides three input, three output leads, two power leads and a ground, plus three miscellaneous terminations.

4.7 Interconnection — Jumper Wafers

4.7.1 Each 28/20 ICM Module design contains an end wafer, a jumper wafer, or a combination interconnection-jumper wafer. Figure 4-8 shows a typical 28-notched wafer configuration. Two types of material are being considered:

(a) a 20 mil thick printed circuit wafer (epoxy) with plated-through notches and staggered pad areas on alternate surfaces,

(b) a 10 mil thick ceramic wafer.

Request for Quotations have been placed with several vendors to obtain cost comparisons, as well as, delivery particulars. In order to expedite the program, a small order has been placed for printed circuit type end wafers to evaluate the metallization of the epoxy in meeting the 500 gram pull test requirements.

Figures 4-9 and 4-10 illustrate the interconnection patterns of the basic Interconnection-Jumper Wafer layouts. Types J-1 and J-2 are being used to perform all the interconnection functions and end tie-points of the four (4) types of ICM Modules for this program.

4.8 Module Performance Specifications

The performance specifications for the four module types will be based on the capabilities of Fairchild's Micrologic II elements. Since only the service leads, i.e. V_{CC} and Ground are interconnected in the module, Fairchild's published data can be used for testing the modules.

The performance of the ICP's in the module assembly may reflect differences in distributed capacitance as compared to Fairchild testing setting-up. Such differences are best evaluated through measurement of the completed modules.

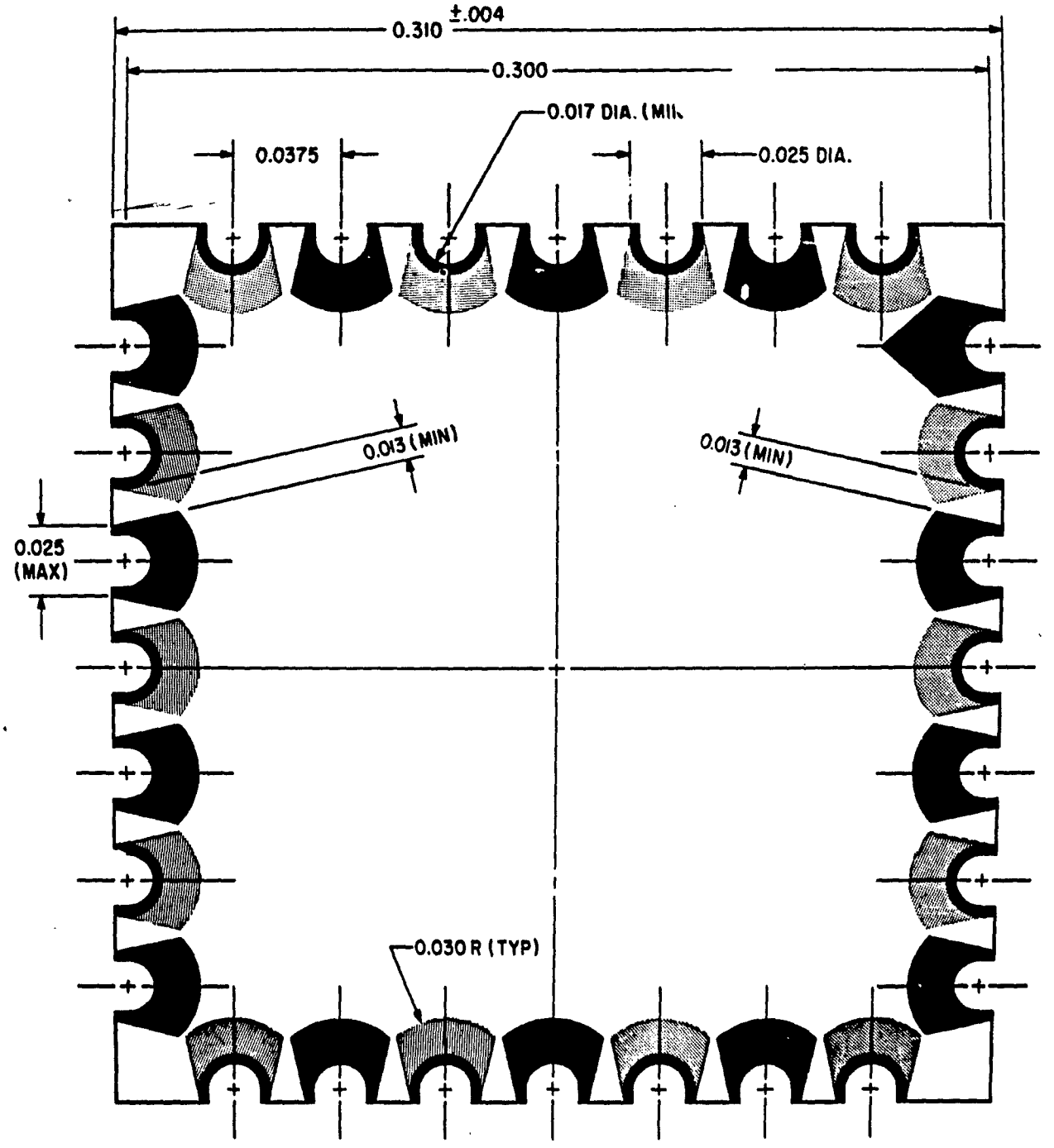


Figure 4-8. End Wafer

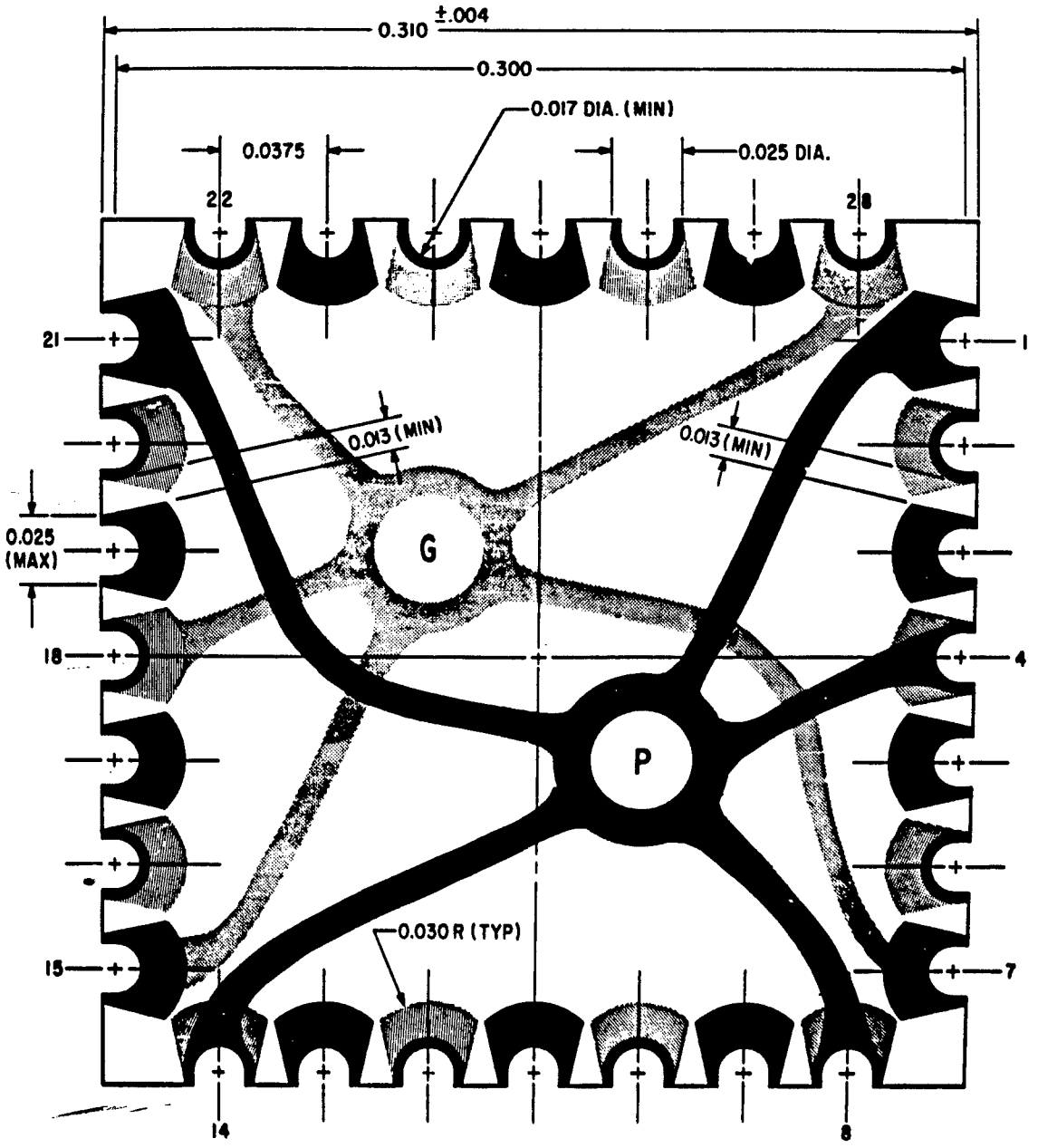


Figure 4-9. Interconnection-Jumper Wafer (J-1)

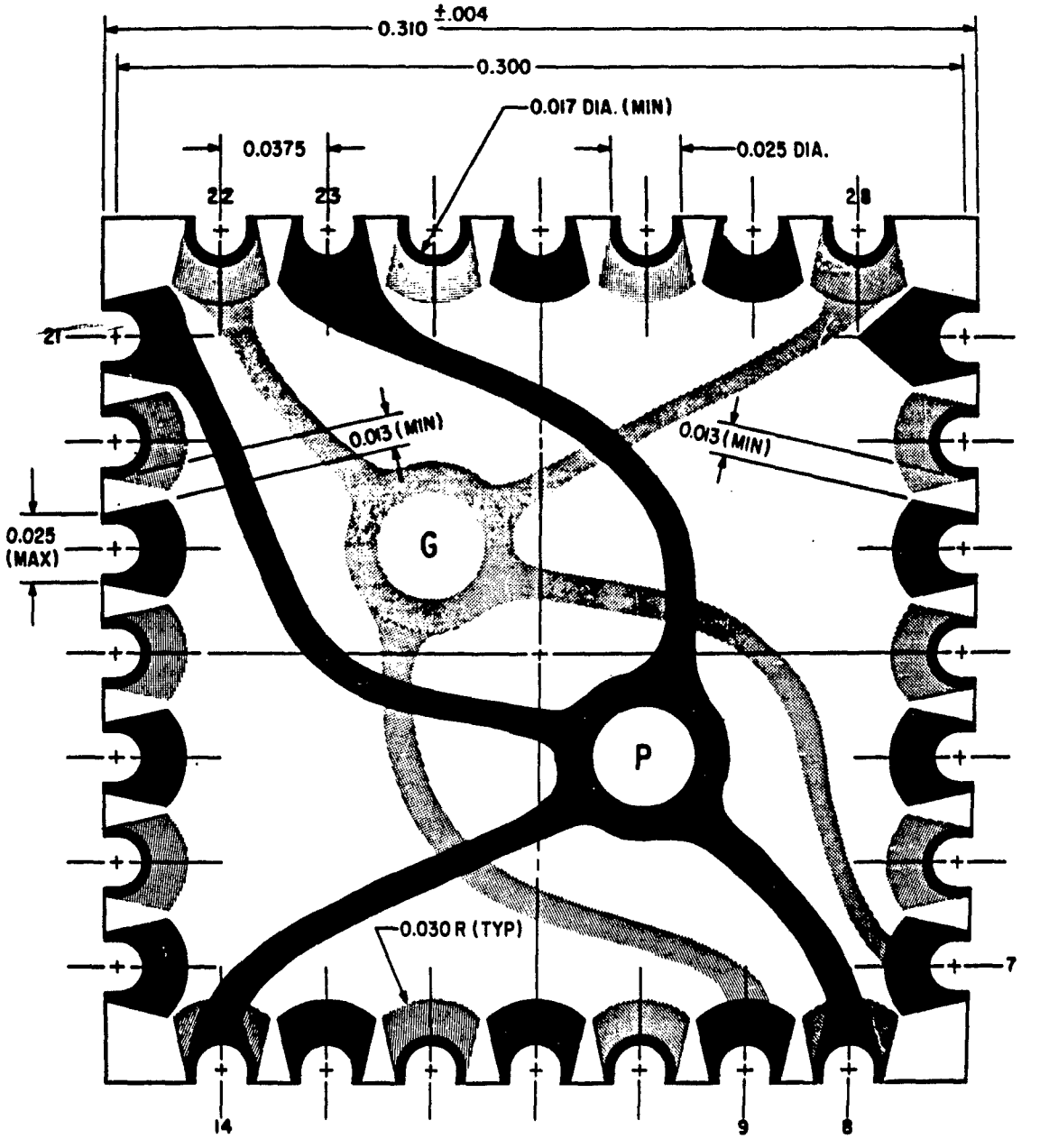


Figure 4-10. Interconnection-Jumper Wafer (J-2)

5.0 CONCLUSIONS

The 28/20-Module Assembly promises to satisfy the low cost objectives of this program. This is based on the fact that standard logic element monolithic devices are available in suitable flat packages, instant compatibility of ICP and module is obtained by substituting a special lead frame in the vendors standard product.

By careful allocation of lead functions in a module universal type modules can be developed which have fewer types than the variety of ICP's (4 vs 6). Each module employs only one of two standardized interconnection wafers.

The logic content of the 28/20 Module Assembly has a density of at least five times greater than the standard 12 lead micromodule.

6.0 PROGRAM FOR NEXT QUARTER

(1) Order logic elements, wafers printed circuit etc., and assemble the 28/20-modules and MICRORAC functional assembly.

(2) Evaluate different materials for use as interconnection wafers.

(3) Test and Evaluate Modules and MICRORAC Functional Assembly.

(4) Complete Survey of Monolithic Silicon Devices.

7.0 IDENTIFICATION OF KEY PERSONNEL

During the quarter, the following personnel took part in the work.

Name	Title	Hours
P. Margolin	Project Leader	160
A. Krell	Design Engineer	390
A. M.M. Hoque	Design Engineer	30

One engineer identified below has been added during the quarter.

A. M.M. Hoque

Mr. Hoque is a graduate of the Govt. College, Rajshahi, E. Pakistan, with the degree of Intermediate of Science (1952); the University of Dacca, E. Pakistan, with a BSc (Honors in Physics) (1952) and a MSc (Physics) (1953). He also holds a MSEE from Polytechnic Institute of Brooklyn (1958).

Mr. Hoque joined RCA in Mobile Communications in July 1958. He worked on selective calling system by phase-modulating the carrier by different tone. He redesigned commercial mobile communication systems for BMEWS, and also designed a 30-watt, 150 mc transmitter using direct heating filament type pulses. Mr. Hoque was also responsible for the design of the front end of a transmitter providing 75 mc driver using transistors.

In 1960 he transferred to Microwave Communications where he worked on up-converters.

Subsequently, Mr. Hoque transferred to EDP where he performed a comprehensive mathematical analysis for various types of mismatched transmission lines, worked on power distribution to logic gates at 300 mc, and made studies on the merits and demerits of 4-phase and 3-phase locked-pair tunnel diode systems.

All the mathematical analyses were carried on and programmed for the IBM 709 computer. Mr. Hoque has worked extensively on computers, their logic and programming.

More recently, he carried out a comprehensive analysis on the sensitivity and reliability of various equalizers used in SAC/CTE on the IBM 709. A complete study on non-ideal transmission lines of SAC having non-ideal equalizers was made in the Communications Systems Division.

Mr. Hoque has been developing microelectronic devices and modules since July 1963.

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Unclassified report

The selected functional assembly of the MICRORAC computer, the Timing Level Generator, was analyzed; and four module types were developed to satisfy its requirements. The modules contain either 2, 3, or 4 Integrated Circuit Packages and one interconnection wafer. A new Integrated Circuit Package having 14 leads was developed as a compatible unit for assembly into the new module. Each terminal of the package connects with an alternate riser wire of the module. Design rules are established for allocating pin functions in the 2s/2o module, for allocating terminal leads of the integrated circuit packages, and for employing intramodule interconnection wafers. Results indicate that the 2s/2o module assembly will satisfy the low-cost objective of this program, because standard logic-element monolithic devices are available in suitable flat packages; and instant compatibility of the integrated circuit package and module is obtained by substituting a special lead frame in the vendor's standard product. Each module employs only one of two standardized interconnection wafers. The logic content of the 2s/2o module assembly has a density of at least 5 times greater than the standard 12-lead micromodule.

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3. Microminiaturization - Integrated Circuit Packaging

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